



DS-03-015

February 9, 2004

To: Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
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Subject: | Serial No. 10/706,837 11/12/03 |

Dr. Axel Pannwitz

FREQUENCY COMPENSATION SCHEME FOR  
LOW DROP OUT VOLTAGE REGULATORS.  
USING ADAPTIVE BIAS

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
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mail in an envelope addressed to: Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450, on February , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 2/12/04

Co-pending U.S. Patent Application serial number 10/347,983 (DS-02-025) filed 01/21/03 to the same assignee, "Regulated Cascode Structure for Voltage Regulators," describes a LDO having an error amplifier as part of a current mirror output stage.

U.S. Patent 6,246,221 to Xi, "PMOS Low Drop-out Voltage Regulator Using Non-inverting Variable Gain Stage," describes a high power supply ripple rejection (PSRR) internally compensated low drop-out (LDO) voltage regulator using an output PMOS pass device.

U.S. Patent Application Publication US 2002/0130646 A1 to Zadeh et al., "Linear Voltage Regulator Using Adaptive Biasing," describes a linear voltage regulator, such as a low-dropout regulator, supplying power to one or more digital circuits within a computer system.

U.S. Patent 6,518,737 to Stanescu et al., "Low Dropout Voltage Regulator with Non-Miller Frequency Compensation," discusses a low dropout voltage regulator with non-Miller frequency compensation.

Sincerely,



Stephen B. Ackerman,  
Reg. No. 37761

Doctor Number (Operator)	Application Number
DS-03-015	10/706,837
Applicant	Dr. Axel Pennwitz
Filing Date	11/12/03
Group Art Unit	

01 INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION

FEB 17 2004 (Use several sheets if necessary)

U. S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

**OTHER DOCUMENTS** (Including Author, Title, Date, Portion or Pages, Etc.)

- Co-pending U.S. Patent App. Serial # 10/347,983 (DS-02-025), filed 01/21/03, same assignee, "Regulated Cascode Structure for Voltage Regulators," U.S. Patent App. Pub. US2002/0130646 A1 to Zadeh et al., Pub. Date 9/19/02, US Class 323/275, Filed 8/28/01.

**EXAMINER**

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.